SCHOTTKY DIODE WITH HIGH FIELD BREAKDOWN AND LOW REVERSE LEAKAGE CURRENT

Field of the Invention

[0001] The present invention relates to a Schottky diode semiconductor devices, specifically, to a Schottky diode device having less leakage current and high field breakdown and a method of manufacturing the same.

Background of the Invention

[0002] Schottky diodes are widely used as voltage rectifiers in many power switching applications, such as switching-mode power supplies, electric motor, switching of communication device, industry automation and electronic automation and so on. Though the Schottky diodes have a high speed switching characteristics, the large reverse leakage current and low breakdown voltage will limit the operation of Schottky diodes to a high reverse voltage and with a higher temperature.

[0003] It is well known that a p+ guard ring diffusion region surround the periphery of the active Schottky contact area could increase the reverse breakdown voltage (U.S. Patent 3,541,403). The p+ guard ring diffusion region is formed from boron-nitride diffusion source or by boron or BF_2^+ ion implantation. However, the high dose boron ion implantation will induce

surface damage and result in high leakage current. Also, the p-n junction curvature effect, referred to S. M. Sze: "Physics of Semiconductor Devices", 2nd, Chapter 2, will significantly affect the reverse leakage current and breakdown voltage. It needs a very long term thermal cycle at high temperature to drive in the boron dopant deep enough into silicon substrate to form a large p-n junction curvature to reduce the reverse leakage current and increase the breakdown voltage.

[0004] An object of the present invention is to propose a new method of forming a high switching speed Schottky diode with high breakdown voltage and low leakage current.

Summary of the Invention

[0005] A Schottky diode structure and a method of making the same are disclosed. The method comprises following steps: firstly, an n+ semiconductor substrate having a first conductive layer and an n- epi layer is provided. Then a first oxide layer is formed on the n-epi layer. A patterning step to define guard-ring (GR) regions and the first oxide layer at this region is etched out. After stripping the photoresist, a polycrystalline silicon layer is deposited by LPCVD or APCVD. Then, the boron or BF_2^+ ion implantation is performed. Thereafter, a high temperature annealing process to drive in the boron ions through the polycrystalline silicon layer into the n- epi layer is carried out using the doped polycrystalline silicon layer as a diffusion source. Subsequently, an oxidation process to fully oxidize the

polycrystalline silicon layer into thermal oxide and drive in the boron ions deep into silicon substrate is then performed. A second mask and etch steps are then implemented to open the active area (AA) regions. A barrier metal deposition and metal silicidation process is then done. After the top metal formation, the third mask and etch steps are then implemented to define the anode. Finally, a backside metal layer is then formed and served as a cathode.

Brief Description of the Drawings

[0006] The foregoing aspects and many of the attendant advantages of this invention will become more readily appreciated as the same becomes better understood by reference to the following detailed description, when taken in conjunction with the accompanying drawings, wherein:

[0007] FIG. 1A to FIG.1C show conventional processes for Schottky diode devices with p+ guard rings.

[0008] FIG. 2 is a cross-sectional view illustrating a patterning process to defined guard rings by using a first photoresist pattern in accordance with the present invention.

[0009] FIG. 3 is a cross-sectional view of forming a polycrystalline silicon layer on all regions and then performing blanket boron or BF_2^+ ion implantation in accordance with the present invention.

[0010] FIG. 4 is a cross-sectional view of performing an annealing process to form p+ buried region by using the doped polycrystalline silicon layer as a diffusion source in accordance with the present invention.

[0011] FIG. 5 is a cross-sectional view of oxidizing the polycrystalline silicon layer into thermal oxide and driving in boron ions deep into the silicon substrate in accordance with the present invention.

[0012] FIG. 6 is a cross-sectional view of forming a second photoresist pattern to define the active region in accordance with the present invention.

[0013] FIG. 7 is a cross-sectional view of etching those exposed oxide layers and then forming silicide layer on active region and then forming a top metal layer and then patterning the top metal layer for forming an anode electrode in accordance with the present invention.

[0014] FIG. 8A and 8B show synoptic layouts of the devices in accordance with the present invention.

[0015] FIG. 9 is a cross-sectional view of Schottky diode structure having the plurality of guard rings at the active region and two at the termination regions according to the present invention.

Detailed Description of the Preferred Embodiment

[0016] The preferred embodiment is to illustrate the method of forming termination structure and the Schottky diode simultaneously.

[0017] Referring to FIG.2, a cross-sectional view shows a semiconductor substrate 100 having a relatively heavily doped n+ doped layer 101 and a lightly doped n-epi-layer 102 provided.

[0018] A thick oxide layer 110 between about 100 to 2000 nm is then formed on the n-epi layer 102 by a thermal oxidation process or by using CVD technique. A photoresist pattern115 having openings 115A to define guard ring regions is then formed on the first oxide layer 110.

[0019] Still referring to FIG.2, an etching step is then performed to etch the first oxide layer 110 by using the photoresist pattern 115 as a mask. The photoresist pattern 115 is then stripped away.

[0020] Afterward, referring to FIG.3, a polycrystalline silicon layer 140 between about 20 nm to 1000 nm is then formed on all areas by using a process of low pressure chemical vapor deposition (LPCVD). A high dose BF_2^+ or boron ions is blanket implanted into the n-epi layer 102 by using a dosage between about 1E11 to 5E16/cm^2 and energy between 10 to 400KeV, respectively.

[0021] Referring to FIG.4, a high temperature anneal process is then carried out to activate ions and form p+ regions 150 using the polycrystalline silicon layer 140 as a diffusion source.

[0022] Referring to FIG.5, a thermal oxidation process is then performed to grow a second oxide layer 140A by oxidizing the polycrystalline silicon layer 140. Meanwhile, the impurities are driving into the n-epi layer 102 by both lateral and longitudinal diffusion to expand

buried p+ region 150 thereof. The expanded p+ regions herein are also called guard rings 165.

[0023] Subsequently, please see FIG.6, a photoresist pattern 160 having openings to expose an active region is formed. The active region includes a region from a portion of guard ring 165 at a termination region 200a to another 200b, and all guard rings 165 in between the termination region 200a and 200b, please also forward to FIG.9.

[0024] Referring to FIG.6, a wet etch is then performed to etch the exposed all of those exposed oxide layer 110, 140A by using the photoresist pattern 160 as a mask.

[0025] As is shown in FIG.7, after stripping away the photoresist pattern 160, A Schottky barrier metal layer 170 is then deposited on all areas. The material of the barrier metal for instance, includes Ti, Ni, Cr, Pd, Pt, W, Mo etc. A thermal anneal at a temperature between about 200 to 850 °C in nitrogen ambient is then done to form a silicide layer 170 on the active regions.

[0026] The unreacted metal layer on the second oxide layer140A is then removed. Afterward, another thick top metal layer 180 is then formed on the entire areas. An exemplary candidate for the top metal layer is a Ti/Ni/Ag or Ti/Ni/Al layer, etc. Afterward, the top metal layer 180 is patterned to define anode. The resulted top metal layer 180 covers the entire active region and is extended to a portion of termination mesa region. Subsequently, a lapping process is performed firstly to remove all of the layers formed on the backside surface of the substrate 100 during

aforementioned processes and then a backside metal layer 190 acted as a cathode is formed thereafter by sputtering.

[0027] FIG. 8A and 8B show synoptic layouts of the devices in accordance with the present invention. It shows a plurality of square guard rings165 or rectangular guard rings165.

[0028] FIG .9 shows a cross-sectional view of the device having two guard rings at the active region and two at the termination regions according to the present invention.

[0029] The benefits of this invention are:

[0030] 1. The guard rings p+ region at the termination region is broad and extended and thus the bending region of the depletion boundary far away from the active region than the conventional device.

[0031] 2. The high dose ion implantation damages could be neglected by using the polycrystalline silicon layer as the diffusion source, by referring to the author's other patent: U.S. patent No. 5,347,161. Base on the above benefits, the Schottky diode with high breakdown voltage and low reverse leakage current could be obtained.

[0032] As is understood by a person skilled in the art, the foregoing preferred embodiment of the present invention is an illustration of the present invention rather than limiting thereon. It is intended to cover various modifications and similar arrangements included within the spirit and scope of the appended claims, the scope of which should be accorded the broadest interpretation so as to encompass all such modifications and similar structure.